REMARKS

The Examiner's non-final Office Action of March 19, 2004 has been received and its contents reviewed. Accordingly, claim 1 has been amended, and new claims 7-12 have been added. Claims 1-12 are currently pending with claims 1 and 7 being independent.

Initially, the Applicants wish to thank the Examiner for agreeing, during a telephone conference of May 12, 2004, to permit in the instant application the inclusion of claims 7-12 from parent Application No. 09/984,908 ('908), now U.S. Patent 6,666,577 A1 ('577), for the purpose of considering the references cited in an Information Disclosure Statement (IDS) of December 19, 2003, which were properly filed in the '908 application, with regard to the claims 7-12 (claims 1-6 of the U.S. Patent 6,666,577). It is noted that the Examiner has listed each of the documents cited in the IDS of December 23, 2003 on the PTO-892 form accompanying the outstanding Office Action of March 19, 2004. It is respectfully requested that the Examiner indicate his consideration of the references from the December 19th IDS with regard to the instant claims 7-12 (from the '908 application & '577 patent) by returning to the Applicants with the next Office Action an initialed copy of the PTO-1449A form (from the '908 application) attached hereto.

The Applicants respectfully request reconsideration of the above-identified application, in view of the above amendments and for the reasons to follow.

With regard to the Examiner's formality objections to the specification and drawings, the above amendment to the specification and the attached replacement sheet for Figures 11A and 11B are believed sufficient to merit withdrawal of each of these objections.

With regard to the Examiner's rejections of:

Claims 1, 2, 4 and 6, under § 101, as being the same invention as set forth in claims 1, 2, 4 and 9 of copending Application No. 10/638,062,

Claims 3 and 5, under the judicially established doctrine of obviousness-type double patenting, as being obvious in view of claim 7 of copending Application No. 10/638,062 in combination with the teachings of WO 98/57146,

> Claim 1, under § 102(b), as being anticipated by the teachings of Dutartre ('676),
>
> Claims 1-5, under § 102(e), as being anticipated by the teachings of Johnson ('232), and
>
> Claim 6, under § 103(a), as being obvious in view of the teachings of Dutartre ('676),

each these rejections are respectfully traversed.

Specifically, the Applicants note that a letter of Express Abandonment has been filed in copending Application No. 10/638,062 on April 8, 2004, rendering moot the rejections under § 101 and obviousness-type double patenting.

Additionally, the method of claim 1 for predicting a temperature of a wafer includes the following features:

> ...c) calculating a recovery rate of the second semiconductor layer from the amorphous state to the crystalline state at which a part of the second semiconductor layer that has been heated recovers from the amorphous state to the crystalline state at the interface with the first semiconductor layer; and
>
> d) measuring a temperature of the test wafer that has been irradiated with the light, according to a relationship between the recovery rate and a temperature corresponding to the recovery rate. (Emphasis added)

A review of both the Dutartre and Johnson et al. references reveals that, contrary to the Examiner's assertion, neither reference alone (or in any combination) remotely teaches or suggests the above features. Specifically, the highlighted features refer to "a recovery rate" of the second semiconductor film from the amorphous state to the crystalline state which is clearly defined in the specification as the change in thickness of the second semiconductor layer over time, see page 10, lines 3-20. Thereafter, the temperature can be accurately measured (predicted) from the determined recovery rate, using a known plot of a relationship between the recovery rate and the actual temperature (see Figure 13), which corresponds to a particular temperature.

A review of both the Dutartre and Johnson et al. patents reveals that each employs a correlation between the sheet resistance, i.e., ohms/square, (which is also related to the change in thickness of semiconductor layer as a result of crystallization) and the (change in) temperature. That is, Dutartre teaches, as shown in Fig. 3, a method for calibrating

temperature including the steps of measuring a first sheet resistance with respect to a reference wafer, and performing a heat treatment, thereafter measuring a second sheet resistance and determining the difference in temperature based on the changes in the sheet resistance. Dutartre further teaches (see column 5, lines 16-38) a sequence of measuring a sheet resistance, performing a heat treatment at 1100°C, and measuring a sheet resistance. Since the changes in the sheet resistance is used to determine the temperature in Dutartre, the amended claim 1, which uses the recovery rate of the semiconductor layer from the amorphous state to the crystalline state, is completely different from Dutarte.

The Examiner asserts that the "recovery rate" in the amended claim 1 includes the "changes in the sheet resistance" in Dutartre. However, the "recovery rate" in the amended claim 1 refers to "a recovery rate of the second semiconductor layer from the amorphous state to the crystalline state at which a part of the second semiconductor layer that has been heated recovers from the amorphous state to the crystalline state at the interface with the first semiconductor layer", and is impossible to include the changes in sheet resistance of the test wafer.

Finally, since Dutartre teaches the steps of:

1) implanting ions (amorphous state),

2) crystallizing and annealing in an oxygen ambient,

3) measuring the first sheet resistance,

4) annealing,

5) measuring the second sheet resistance, and

6) determining the changes in the sheet resistance,

and the amorphous state only appears immediately after ions implantation, a semiconductor layer in a amorphous state is certainly not used to determine the temperature.

Similarly, Johnson et al. teach performing an ion implantation on a substrate 32 to form an amorphous region 40 (Figs. 3 and 4), and thereafter loading the substrate 32 into a heating chamber 50 (Fig. 5) and performing a heat treatment to form an amorphous region 42 and a re-crystallized region 44. At this time, the thickness of the amorphous region 42 varies as t1, t2 and t3, and the sheet resistance also differs. Hence, since

Johnson et al., which is the same as Dutartre, merely disclose a method of measuring the temperature based on the sheet resistance, which is completely different from the present invention of using the recovery rate of the second semiconductor layer recovering from the amorphous state to the crystalline state, the present invention is also different from that of Johnson et al.

For the above reasons, the rejections of claims 1-6, under § 102 or § 103(a), based upon the teachings of Dudartre or Johnson et al. are no longer appropriate and must now be withdrawn.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,

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